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For: **INTEGRATED MODULATORS AND DEMODULATORS**

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Enclosed is a certified copy of British Appln. No. 0219740.8 filed on August 23, 2002, from which priority is claimed under 35 U.S.C. §119.

Respectfully submitted,

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	Patents ADP number *(if you know it)*	07341362003
	If the applicant is a corporate body, give the country/state of its incorporation	Republic of Korea
4.	Title of the invention	Integrated Modulators and Demodulators
5.	Name of your agent *(if you have one)*	RGC Jenkins & Co
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Integrated Modulators and Demodulators

This patent application relates to the field of data transfer. More particularly, but not exclusively, it relates to a modem for data transfer, which is capable of modulating or demodulating data using multiple modulation techniques.

In order to transmit information or data from one point to another or from one device to a second device, either via a communication line or a wireless link, data are transformed into a suitable form for being transmitted, typically by putting it onto a carrier. This is called modulation. After the data have been received by the second device, the modulated data are "demodulated", i.e. removed from the carrier and brought back into a suitable form for future use of the second device.

More and more devices are designed to communicate with each other, for example via a local area network (LAN). For wireless LANs, different modulation standards have been introduced for ensuring compatibility such as the IEEE 802.11 standard. A similar concept for data transmission, but more for Personal Area Networking (PAN), can be seen in the BluetoothTM standard.

Devices capable of communicating with other devices via a particular modulation technique each include a modulator and/or a demodulator, which is particularly designed for modulating/demodulating data according to the particular modulation technique. Referring now to Figure 2, a modem 30 is

illustrated, including a modulator 32 and a demodulator 34. The modulators and demodulators for different modulation techniques can differ considerably from each other.

If one particular device is designed to be capable of communicating using two different standards, for example the IEEE 802.11 and the Bluetooth standard, the approach adopted in the prior art is to use a combined modem including two separate modems, wherein each of these separate modems works according to one modulation technique. Such a modem is illustrated in Figure 3. The modem 40 includes two separate modems 41 and 47. Modem 41 comprises modulator 42 and demodulator 44, whereas the modem 47 comprises modulator 43 and demodulator 45. The first modulator 42 and the first demodulator 44 are specific to the IEEE 802.11b technique and the second modulator 43 and the second demodulator 45 are specific to the Bluetooth standard. In addition to the two modems an additional switching and interworking element 46 is required, which ensures that data are modulated according to the desired standard for a particular application and that incoming modulated data are correctly demodulated. The interworking element 46 also ensures that each modem pair are correctly updated with control information to ensure that any switching between modems also has the correct timing alignment and correct control procedures are carried out.

It is an aim of the present invention to improve the system described above.

According to one aspect of the present invention there is provided a modulating device comprising means for modulating and/or demodulating data for transmission, wherein the modulating means is capable of modulating and/or demodulating data according to at least a first and a second modulation technique using common digital modulation components.

Preferably, the modulating means comprises a plurality of building blocks and wherein at least one of said building blocks are adapted to be used to modulate data according to said at least first and second modulation technique.

The first technique may involve quadrature modulation and the second may involve frequency modulation.

In this way a more efficient use of modem modules is ensured by avoiding duplication of modulation and/or demodulation modules. The integrated modem comprises a single modulator and single demodulator. This integrated architecture performs the integration at a deeper level than the conventional way of simply including two separate modems and switching/interworking between the two as appropriate. Lighter and smaller designs of devices become possible which provide compatibility of more than one communications standard. If less space is occupied by the modem, other functional elements, like for example additional memory, can be inserted.

Preferably, a modulating means wherein said modulating means is adapted to automatically switch between said first and second mode.

In this way, no additional switching/interworking element is required. Less hardware and code is needed to provide multiple modem functionality, and the complexity of the system can be reduced compared to the prior art solution.

Further aspects and advantages of the invention will be appreciated, by way of example only, from the following description and accompanying drawings, wherein:

Figure 1 is a schematic outline of elements used for communicating of digital data in a communications system;

Figure 2 is a block diagram of a modem in which the present invention can be implemented;

Figure 3 is a block diagram of a modem according to the prior art;

Figure 4 illustrates CCK code word generation;

Figure 5 is block diagram illustrating a CCK+DQPSK modulator according to the prior art;

Figure 6 is a block diagram illustrating a serial-to-parallel converter for the modulator of Figure 5;

Figure 7 illustrates an example of input and output data of the serial-to-parallel converter of Figure 5;

Figure 8 illustrates an alternative means for code word derivation used in the modulator of Figure 5;

Figure 9 is a block diagram illustrating the differential modulator 130 of Figure 5;

Figure 10 is a block diagram illustrating a CCK+DQPSK demodulator according to the prior art;

Figure 11 is a block diagram illustrating a complex correlator 210 of Figure 10;

Figure 12 is a block diagram illustrating a GFSK modulator according to the prior art;

Figure 13 illustrates Gaussian outputs according to the GFSK modulation technique;

Figure 14 is a block diagram illustrating a GFSK demodulator according to the prior art;

Figure 15 is a block diagram illustrating a matched filter implemented in an FIR architecture;

Figure 16 is a block diagram illustrating an integrated modulator according to one embodiment of the present invention; and

Figure 17 is a block diagram illustrating an integrated demodulator according to one embodiment of the present invention.

Referring now to Figure 1, the elements typically used for communicating digital data between two devices are shown.

The transmission process 10 comprises a source coder 12, a channel coder 13, a modulator 14, an up-converter 15 and a power amplifier 16. The receiver line 20 comprises a low noise amplifier 26, a down-converter 25, a demodulator 24, a channel decoder 23 and a source decoder 22.

The data to be transmitted are provided, in a suitable digital form, to source coder 12 (e.g. a voice codec such as an LPC coder, or an image codec such as a JPEG or MPEG coder), which removes information redundancy. The output of the source coder 12 is ideally an uncorrelated data stream, which is represented by fewer bits than the originally provided data stream. In channel coder 13 (e.g. a Viterbi or turbo coder), the data are prepared such that channel errors can be detected and/or corrected at the receiver. This is achieved by the channel coder 13 adding redundancy which enables the receiver to detect and/or correct possible errors.

Modulator 14 transforms the data into a form suitable for transmission. Digital modulation can usually be divided into two parts – the first part involving digital processing of the incoming bit stream and the second part involving the conversion of the resulting processed data into an analogue form, for transmission, for example over the air.

In up-converter 15 the data are translated to the frequency where bandwidth has been allocated for the transmission, and the output original strength is subsequently enhanced in power amplifier 16 such that the power is sufficient to transmit the data to the receiving device.

On the receiver line 20, the data received are first amplified in a low noise amplifier 26. The data have been attenuated through the transmission from one device to another and are therefore enhanced in low noise amplifier 26 such that they are at a level suitable for further handling at the following

elements of the receiver line 20. This amplifier does not add any further significant noise to the received data.

The downconverter 25 then moves the data signals from their allocated transmission bandwidth to a predetermined baseband. In demodulator 24, the process of modulation carried out in the transmitter is converted back into a digital form.

In the channel decoder 23 errors which occurred during transmission of the data via the transmission channel are detected and corrected. The output from the channel decoder 23 is then brought into a form required by the point of reception at a source decoder 22.

Referring now to Fig. 2, a device capable of communicating using a particular modulation technique comprises a modem 30, i.e. a modulator 32 and a demodulator 34, specifically designed for modulation and demodulation according to that particular modulation technique.

There are many different forms of digital modulation/demodulation.

Complementary Code Keying (CCK) with Differential Quadrature Phase Shift Keying (DQPSK), referred to as CCK+DQPSK in the following, is for example used in the IEEE802.11b standard. Gaussian Frequency Shift Keying (GFSK) is for example used in the Bluetooth™ standard.

In the following the principles of CCK+DQPSK keying are described.

Complementary Code Keying with DQPSK Description

Complementary Code Keying (CCK). CCK is designed to increase underlying user data rates while maintaining user bandwidth.

More details may for example be found in IEEE 802.11 b-1999 standard, or in M. Webster, C. Anderson, J Boer and R. Van Nee: "Introducing the Harris-Lucent Compromise Proposal for TGb", doc: IEEE P02. 11-98/246 & 232, 1998, C. Andren, M. Webster and K. Halford: "CCK, the New IEEE 802.11 Standard for 2.4 GHz Wireless LANs" or C.Andren and M. Webster: "A 2.4 GHz 11 Mbps Baseband Processor for 802.11 Applications", 2002.

Code words used in CCK modulation are called complementary codes. Complementary codes have low crosscorrelation and good autocorrelation properties.

CCK as described herein encodes 8 bits of information in a single code word, and the ratio of information bits encoded to number of output chips is 1:1. CCK is a form of M-ary orthogonal keying modulation in which one of a set of M unique code words is chosen for transmission based on the information bits at the input of the modulator. A CCK code word is 8 complex chips in length, and the choice of code word to be transmitted is dependent on:

(a) the 8 information bits at the input of the modulator;

(b) the previously encoded code word; and

(c) whether the symbol (8-chips) occupies an even or odd (data bit) position in the output data stream.

The encoding of the 8-bit word $d_0d_1d_2d_3d_4d_5d_6d_7$ is described in the following.

The first dibit d_0d_1 is encoded using DQPSK. In this way there is a phase change $\Delta\theta$, i.e. a change in phase between the actual phase value θ and the phase θ' of the previous code word. Depending on the position in the output data stream, ie whether the data occupy an even or odd position, different values for the phase change $\Delta\theta$, are associated to the dibit d_0d_1. The DQPSK encoding table used for encoding the first dibit is shown in Table 1.

Dibit pattern (d_0d_1)	Even symbols phase change in θ_1 (i.e. $\Delta\theta_1$)	Odd symbols phase change in θ_1 (i.e. $\Delta\theta_1$)
00	0	π
01	$\pi/2$	$-\pi/2$
11	π	0
10	$-\pi/2$	$\pi/2$

Table 1: DQPSK Encoding Table

The remaining dibits are encoded using QPSK. A phase θ_2, θ_3 and θ_4 is associated with dibits d_2d_3, d_4d_5 and d_6d_7, respectively, according to the QPSK encoding table shown in Table 2.

Dibit pattern (d_id_{i+1})	Phase (θ_x)
00	0
01	$\pi/2$
10	π
11	$-\pi/2$

Table 2: QPSK Encoding Table

The CCK code word $C_0C_1C_2C_3C_4C_5C_6C_7$ is then built according to table 3 using the complex symbols $\exp(j(\theta_1))$, $\exp(j(\theta_2))$, $\exp(j(\theta_3))$ and

exp(j(θ_4)), using the phases θ_1 to θ_4 as obtained from the QPSK dibit encoding described above.

The CCK code word determination is illustrated in Figure 4.

The first dibit d_0d_1, is DQPSK modulated, resulting in a phase θ. The second to fourth dibits d_2d_3, d_4d_5 and d_6d_7 are QPSK encoded. The CCK code word building using QPSK encoding in phases θ_2, θ_3 and θ_4 can be interpreted as modulating every odd chip, every odd pair of chips and every odd quadruple of chips, respectively, as can be seen in Table 3 and Figure 4.

Code word Element	Value
C_0	exp (j(θ_1+ θ_2+θ_3+θ_4)
C_1	exp (j(θ_1+ θ_3+θ_4)
C_2	exp (j(θ_1+ θ_2+θ_4)
C_3	-exp (j(θ_1+θ_4),
C_4	exp (j(θ_1+ θ_2+θ_3)
C_5	exp (j(θ_1+ θ_3)
C_6	-exp (j(θ_1+ θ_2)
C_7	exp (j(θ_1)

Table 3: CCK Code word

INPUT DATA WORD $d_2d_3d_4d_5d_6d_7$	**OUTPUT CODE WORD** $c_0\ c_1 c_2\ c_3\ c_4\ c_5\ c_6\ c_7$
0 0 0 0 0 0	+1+1+1-1+1+1-1+1
1 0 0 0 0 0	-1+1-1-1-1+1+1+1
: : :	: : :
1 1 1 1 1 1	+j-1-1+j-1-j+j+1

Table 4: CCK Code word look-up table

In contrast, θ_1 modulates every chip, i.e. every code word element C_0 to C_7 includes the factor $\exp(j(\theta_1))$. Thus, the effect of including the information of the first dibit is a phase rotation of the complex chip word which is built using QPSK encoding.

CCK +DQPSK modulator

In the following a CCK modulator is described with reference to Figure 5.

The CCK modulator 100 comprises a serial-to-parallel converter 110, a look-up table 120 and a differential modulator 130.

In a first step, incoming data are serial-to-parallel converted into eight parallel data lines. As an example, the rate of the input data is 11 MHz, whereas the output is clocked at 1.375 MHz.

Figure 6 shows a Serial-to-parallel converter 110 including a shift register comprising 7 delay lines 111. The output of the converter 110 are bits d_0 to d_7 on lines 112 to 119, respectively.

Figure 7 illustrates an example of the input data to Serial-to-parallel converter 110 and the output data (line 0 to line 7). After an 8-bit period the state of the output lines reflects the last 8 bits of the input data.

The first two bits d_0 and d_1 of each 8-bit period are directly used as an input to the differential modulator 130, which will be described below.

The remaining bits d_2 to d_7 of the 8-bit period (i.e. bits 3 to 8) are transmitted in parallel to the look-up table 120. The look-up table 120

includes 64 unique 8-chip code words for mapping the incoming 6 bits onto an associated code word.

The code words are built as described above with reference to tables 2, 3. However, the first two bits d_0 and d_1 are not used in look-up table 120, as they are directly transmitted from Serial-to-parallel converter 110 to differential modulator 130. The code word derivation used for the encoding bits d_2 to d_7 is illustrated in Figure 8. Table 4 illustrates the content of the look-up table 120 on a few examples. In the left-hand column input data words are given, and in the right-hand column the associated output code words are listed as obtained using the rules of table 3 illustrated in Figure 8.

The look-up table is implemented in a read-only memory (ROM). For a particular 6 bit input data word $d_2d_3d_4d_5d_6d_7$ a complex 8-chip code word $C_0C_1C_2C_3C_4C_5C_6C_7$ can be derived.

As the code words are complex, two output lines 122 and 124 are provided. The real parts are placed on an inphase line 122, whereas the imaginary parts are placed on a separate quadrature line.

The output of element 120 and the two bits d_0 and d_1 are fed to differential modulator 130.

Figure 9 illustrates differential modulator 130, comprising elements a look-up table 135, computational element 136, memory 131, and element 137 for rotating the complex chip by an angle determined by computational element 136.

In a first step, the differential modulator 130 stores the phase θ' (i.e. θ_1 of the previous 8-chip code word) in memory 131. The differential modulator then determines the phase θ_1 of the current 8-chip code word based on the input data bits d_0 and d_1 according to the DQPSK encoding shown in table 1 Computational element 136 subsequently computes the phase difference $\Delta\theta_1$ between the phase θ' of the previous 8-chip code word stored in memory 131 and the phase θ_1 of the current code word. Element 137 then rotates the complex chips word as received in input lines 122 and 124.

Thus the differential modulator 130 encodes the first two bits d_0 and d_1 according to the DQPSK modulation described above and adds the information to the 8-chip code word obtained from look-up table 120. The effect of the CCK modulation of bits d_0 and d_1 is a rotation of the code word about phase difference $\Delta\theta_1$.

The output of differential modulator 130 is the real and imaginary part of the 8-chip code word on output lines 132 and 134, respectively.

CCK+DQPSK demodulator

In the following, a CCK+DQPSK demodulator is described with reference to Figure 10.

The demodulator 200 comprises a matched filter 202, a logic circuit 204, a shift register 206, computing means 208, a bank of 64 correlators 210, a DQPSK demodulator 212, and decision element 214.

In the CCK+DQPSK demodulator 200 the received signal is transmitted to the matched filter 202 to compensate for varying channel characteristics. Matched filter 202 may be combined with a band limiting filter.

Logic circuit 204 determines the global phase rotation θ_1 of the code word by examining the last chip of the complex code word.

It can be seen from Figure 10 that only 64 correlators are used in the demodulator, yet there are 256 (2^8) possible code words that might be received. This is because the 64 initial code words from the modulator look-up table may be given an **initial** rotation of 0, $\pi/2$, π, or $3\pi/2$ radians. The demodulator may thus store the 4 different sets of 8-chip code words (Z_i) to correspond to each possible additional phase shift. The logic circuit is used to determine which set of stored 8-chip code words is to be used in the correlator.

Shift register 206 is also used to introduce a 7-chip delay prior to the correlator bank.

The DQPSK demodulator 212 computes the phase change between the current chip sequence and the previous one. A DQPSK constellation map is then used to decode the information in order to obtain the decoded bits b_0 and b_1.

As seen in the demodulator block diagram of Figure 10, a bank of 64 complex correlators is used to demodulate the CCK signal.

Each received 8-chip sequence is correlated with the 64 stored signals corresponding to the 64 possible 8-chip code words. The code word with the highest correlation is selected, indicating the best match between the received 8-chip sequence and the stored 8-chip code word, in order to decode the transmitted sequence and restore the original information.

Referring now to Figure 11, a complex correlator 210 as used in the demodulator of Figure 10 is illustrated. The complex correlator 210 comprises two simple correlators, one for the inphase arm and the other for the quadrature arm; these are used to correlate the real and imaginary parts of the received chip sequence respectively, and each of the resulting correlations are then added together in adder 229.

The real and the imaginary part of the input signal are sent to the correlator on input lines 222 and 224, respectively. The correlator 210 receives the data Z_i on lines 223 and 224, containing information on which set of code word (corresponding to the determined phase θ_1) is to be used to determine the correlation. The correlation between the stored and received signals is then performed by the 16 correlators 226, together with shift register 227 and computing means 228 and 229.

As seen in Figure 10, decision element 214 receives the outputs from the bank of 64 correlators. Element 214 includes a sampler, a comparator and a decision circuit.

The sampler estimates the amplitude of the signal received from the output of each correlator, and the comparator determines the largest sample.

Decision element 14 stores all possible 6-bit data word containing bits b_2 to b_7. Based on the result from the comparator, the decision circuit outputs the data word associated with the received data. This 6-bit data word together with the two bit word b_0b_1 recovered by the DQPSK demodulator 212 is then the output from CCK+DQPSK demodulator 210 and corresponds to the demodulated transmitted data.

The whole process of demodulation is then repeated for the next and all following 8-chip sequences in an ongoing, continuous process for the duration of communications.

GFSK Modulation

In the following GFSK modulation is described. Further details may for example be found in Steele and Hanzo in ["Mobile Radio Communications", Wiley, 1992], and Watson in ["FSK Signals and Demodulation", 1980].

Binary GFSK is a variation of BFSK (binary frequency shift keying). In BFSK, the binary bit 1 is mapped onto the baseband pulse +1, and the binary bit 0 is mapped onto the baseband pulse –1. The baseband pulses are frequency modulated according to Equation (1a) in which b represents the baseband pulse. Hence, the tones $S_1(t)$ and $S_2(t)$ signal bit 1 and 0 respectively, as seen in equations (1b) and (1c).

$$S(t) = A \cos(2\pi(f_c + b\Delta f)t + \theta) \qquad (1a)$$

$$S_1(t) = A\ \mathrm{Cos}(\ 2\pi(f_c + \Delta f)t + \theta\ ) \quad (1b)$$

$$S_2(t) = A\ \mathrm{Cos}(\ 2\pi(f_c - \Delta f)t + \theta\ ) \quad (1c)$$

GFSK Modulator

Figure 12 is a block diagram of a GFSK modulator. Modulator 300 comprises a single bit shift register 302, a look-up table 304 and a voltage controlled oscillator (VCO) 306.

The function of look-up table 304 is to provide a smooth transition from one baseband pulse to the other in order to bandlimit the transmitted signal. For GFSK, Gaussian transitions are used.

If the signal is bipolar, as for BFSK or binary GFSK, there will be four possible transitions. The look-up table provides Gaussian outputs to the four possible dibit combinations to ensure smooth transitions for all cases. Figure 13 illustrates the four possible GFSK outputs. Table 5 is an example of the actual values stored in a look-up table.

DATA IN (d_{t-1}, d_t)	GFSK table output
00	-1.0000, -1.0000, -1.0000, -1.0000, -1.0000, -1.0000, -1.0000, -1.0000, -1.0000, -1.0000, -1.0000,
10	1.0000, 0.9490, 0.5852, 0.0486, -0.4358, -0.7531, -0.9121, -0.9746, -0.9940, -0.9989, -0.9998
01	-1.0000, -0.9998, -0.9989, -0.9940, -0.9746, -0.9121, -0.7531, -0.4358, 0.0486, 0.5852, 0.9490
11	1.0000, 1.0000, 1.0000, 1.0000, 1.0000, 1.0000, 1.0000, 1.0000, 1.0000, 1.0000, 1.0000,

Table 5: Look-up table for a GFSK modulator.

GFSK modulator receives data on input line 301. The single bit shift register 302 delays one bit, such that two bits are sent simultaneously to the transition look-up table 304. As can be seen from table 5, the GFSK encoding is based on dibit d_{t-1}, d_t.

The output of the look-up table 304 is then transmitted to VCO 306. The VCO transforms the incoming signal by frequency modulation according to equation (1a). The frequency deviation of the transmitted tone is proportional to the amplitude of the baseband signal b. With Gaussian filtering, b is Gaussian distributed about either +1 or –1, thus the frequency is also Gaussian distributed about frequencies f_1 and f_2.

GFSK Demodulator

Referring now to Figure 14, a GFSK modulator is described. The GFSK modulator 400 receives the signal on input 402 and sends it to two matched filters 410. The output of these filters 410 is then sent to decision element 406 for decoding.

Decision element 406 comprises a sampler, a comparator and a decision circuit. Decision element 406 estimates the amplitude of the signal from the output of each filter in a first step. The comparator determines which output is the largest and the decision circuit selects the associated dibit. The output line 404 delivers demodulated data.

Of the matched filters one is matched at frequency f_1 so that it produces the largest output when a bit 1 is received, while the other is matched at f_2 and produces the largest output when a bit 0 is received.

Matched Filters can be implemented using a number of different architectures such as Finite Impulse Response Filters (FIRs) or Infinite Impulse Response Filters (IIRs), cascaded and mixed architectures.

A matched filter realised in an FIR architecture is illustrated in Figure 15. Filter 410 comprises a shift register 412, computational elements 414 and adders 416.

The FIR basic architecture can be used to realise a number of different filter types, for example, Butterworth, Chebychev, Elliptical, Raised Cosine, Root Raised Cosine etc. All have different performance in terms of, for example, cut-off gradiant, ripples in pass-band and stop bands etc. Although they can be realised using the basic FIR architecture each is likely to be of different overall complexity, including making use of cascaded filter stages. In its basic form shown in Figure 15 an appropriate filter design would result in the determination of the FIR filter coefficients or weights b_0 to b_7. It is quite likely to have a larger number of weights than 8.

The input wave form time samples, in the form of Finite Impulses, are fed to the input of the filter. The initial conditions for the filter would be that all outputs from the delay units are set to zero. The output from the filter, after the arrival of the first impulse, i_0, at the filter input would thus be i_0b_0. The second output from the filter, after the arrival of the second impulse, i_1, at the filter input would be $i_0b_1 + i_1b_0$. The third output from the filter, after the arrival of the third impulse, i_2, at the filter input would be $i_0b_2 + i_1b_1 + i_2b_0$ and so on – so that the n_{th} output from the filter after the arrival of the n_{th} impulse,

in, at the filter input would be $i_0b_{(n-1)} + i_1b_{(n-2)} + i_2b_{(n-3)} + \ldots\ldots + i_{(n-3)}b_2 + i_{(n-2)}b_1 + i_{(n-1)}b_0$. The output waveform obtained in this way will be a bandlimited version of the input waveform, i.e. it will be matched to the waveform of interest – the one to be recovered .

The previous two known modulation schemes, i.e. CCK+DQPSK and GFSK modulation, have been described together with possible ways of implementation (i.e. a modulator and a demodulator applying the schemes).

In the following one embodiment of the present invention will be described. This embodiment includes an integrated modulator which is capable of modulating data according to both modulation schemes, CCK+DQPSK and GFSK, and also includes a demodulator capable of demodulating modulated data according to both modulation schemes.

First Embodiment

Integrated Modulator

Referring now to Figure 16, an integrated modulator 500 is described. Similar to the CCK+DQPSK modulator of Figure 5, the modulator 500 includes a serial-to-parallel converter 510, a look-up table 520 and a differential modulator 530. In addition, the modulator 500 also includes a switch 550 and a VCO 540.

Because of the similarities of modulator 100 (of Figure 5) and 500 (of Figure 16), in the following the modulations of modulator 500 compared to the CCK+DQPSK modulator of Figure 5 are described. These modifications

allow the integrated modulator 500 not only to modulate data according to the CCK+DQPSK technique, but also to the GFSK modulation scheme.

The serial-to-parallel converter 510 can be adapted to different timings depending on whether the modulator is used in the CCK+DQPSK or the GFSK mode.

The look-up table 520 is extended such that the GFSK encoding data are also included in the QPSK table.

The following paragraphs describe the changes in more detail.

Serial-to-parallel Converter

From Figures 5 and 12 it can be seen that both CCK+DQPSK, and GFSK require serial-to-parallel conversion. CCK+DQPSK requires this operation in order to group the incoming data bits into 8-bit data words, while GFSK needs serial-to-parallel conversion so that 2 bits, i.e. the current and previous data bit, can be sent to the look-up table simultaneously. The serial-to-parallel converter 510 can achieve both of these operations, as long as the clock speed is adjusted accordingly. Thus, a serial-to-parallel converter with an architecture of converter 110 of Figure 6 is used and means for adjusting timing requirements are added.

For CCK+DQPSK, the data enters the converter 510 at, for example, a rate of 11 MHz, while data leave the converter and are sent to the look-up table 520 at a rate of, for example, 1.375 MHz. In this way, each time the serial-to-parallel converter output is sent to the look-up table 520, the state of the eight parallel output lines reflect the last 8 data bits.

In the GFSK mode, the serial-to-parallel converter 510 sends it output to the look-up table at a rate of, for example, 11 MHz, i.e. at a speed 8 times faster than for the CCK+DQPSK mode.

Serial-to-parallel converter 510 thus needs to be able to handle data at a rate of 11MHz. In the CCK+DQPSK mode the clocking speed needs to be reduced by a factor of 8 compared to the clocking rate of the GFSK mode. This can be achieved by using an additional divider circuit; no additional clock is required.

However, as in the GFSK mode only two databits are handled simultaneously, only the databits d_6 and d_7 of lines 118 and 119 (see Figure 6) are used for GFSK encoding. This can be implemented by either setting all remaining bits d_2 to d_5 to zero or by simply ignoring these bits in the encoding preformed in the extended look-up table 520 (see the description below).

For CCK+DQPSK encoding the serial-to-parallel converter output lines 114 to 119 are used.

Look-up table

Both CCK+DQPSK and GFSK use look-up tables as part of the modulation process. The integrated modulator uses a combined look-up table. Compared to the look-up table used for CCK+DQPSK encoding, an additional column is provided for the GFSK mode. Table 6 illustrates the combined look-up table.

DATA IN	CCK table output	GFSK table output										
$d_2d_3d_4d_5d_6d_7$	$c_0\ c_1 c_2\ c_3\ c_4\ c_5\ c_6\ c_7$	c_0	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}
0 0 0 0 0 0	+1+1+1 -1+1+1-1+1	-1.0000,	-1.0000,	-1.0000,	-1.0000,	-1.0000,	-1.0000,	-1.0000,	-1.0000,	-1.0000,	-1.0000,	-1.0000,
:	:	-	-	-	-	-	-	-	-	-	-	-
0 0 0 0 1 0	-1-1-1+1+1+1-1+1	1.0000,	0.9490,	0.5852,	0.0486,	-0.4358,	-0.7531,	-0.9121,	-0.9746,	-0.9940	-0.9989	-0.9998
:	:	-	-	-	-	-	-	-	-	-	-	-
0 0 0 0 0 1	+j+j+j-j+1+1-1+1	-1.0000,	-0.9998,	-0.9989,	-0.9940,	-0.9746,	-0.9121,	-0.7531,	-0.4358,	0.0486,	0.5852,	0.9490
:	:	-	-	-	-	-	-	-	-	-	-	-
0 0 0 0 1 1	-j-j-j+j+1+1-1+1	1.0000,	1.0000,	1.0000,	1.0000,	1.0000,	1.0000,	1.0000,	1.0000,	1.0000,	1.0000,	1.0000,
:	:	-	-	-	-	-	-	-	-	-	-	-
1 1 1 1 1 1	+j-1-1+j-1-j+j+1	-	-	-	-	-	-	-	-	-	-	-

Table 6: Integrated Modulator Look-up table

The integrated look-up table has three columns. The first column is for the input data code words; it has 64 entries from 000000 to 111111. The next column lists the CCK code words, which are 8 complex chips long, corresponding to each of the data words in the first column.

As described above, the GFSK mode uses only 4 possible dibits, thus the GFSK look-up table has only four lines. The last column of the integrated look-up table therefore requires only four GFSK code words. However, these words need to be placed carefully.

As described above, the serial-to-parallel converter 510 delivers the GFSK output in the GFSK mode on the bit positions d_6 and d_7. Therefore, if the remaining input lines are forced to zero during the GFSK mode, the only possible look-up table inputs used in the GFSK mode are 000000, 000010, 000001, and 000011. Thus in the third column only GFSK code word values are provided for these four input words.

If the remaining bits d_2 to d_5 are not set to zero in the converter 510, the same method can be applied by ignoring in the look-up table all bits in the GFSK mode except the two last bits d_6 and d_7.

In response to the input, the look-up table has the task of providing a smooth (Gaussian) transition from amplitude levels +1 to +1, +1 to –1, -1 to +1, and +1 to +1 respectively.

In the present embodiment, GFSK code word is 11 chips in length so that a clocking speed of 11 MHz will result in a data rate of 1 Mbps. This rate corresponds to the maximum data rate for Bluetooth.

Voltage Controlled Oscillator

In the GFSK mode, the inphase output line 522 is connected to a VCO 540 by switch 550. In this way the Gaussian distributed values received from look-up table 520 are frequency modulated and sent to GFSK output line 570.

In the CCK+DQPSK mode, the VCO is disconnected by switch 550. The data from look-up table 520 are further handled in the differential modulator 530 as described above for the CCK+DQPSK modulator and are subsequently sent to the two CCK+DQPSK output lines 580 and 590.

Integrated Demodulator

Referring now to Figure 17, an integrated demodulator 600 is described.

Similar to the CCK+DQPSK demodulator of Figure 10, the demodulator 600 includes a matched filter 602, a logic circuit 604, a shift register 606, computing means 608, 64 correlators 610, a DQPSK demodulator 612 and decision element 614.

In addition, demodulator 600 includes switching means 605 and a logic circuit 618.

Again, the architecture of the integrated demodulator 600 is based on the architecture of the CCK+DQPSK demodulator of Figure 10. Thus, we will describe in the following only the modification of the demodulator 600 compared to the CCK+DQPSK demodulator of Figure 10.

Switches

Switch 605 is used to switch the demodulator 600 between the GFSK mode and the CCK+DQPSK mode.

CCK+DQPSK demodulation requires a channel matched filter 602, and a seven-bit delay before the correlation procedure starts. This matched filter 602 and delay line 606 are not necessary for GFSK demodulation. Switch 605 is thus included to switch these components off when the demodulator 600 is in GFSK mode. In a similar manner, other parts of the demodulator circuit can be switched on and off dependent on which modulation functionality required, see the description below.

The CCK+DQPSK demodulator of Figure 10 uses a bank of 64 correlators to compare the received code word with stored prototype code words. On the other hand, the GFSK demodulator in Figure 14 uses two filters matched at frequencies f_1 and f_2.

Both functionalities, i.e. the functionality of a correlator for the CCK+DQPSK decoding and the functionality of a matched filter for the GFSK decoding can be performed by an FIR, provided that the weights of the tap delay line are adjustable.

If the FIR filter is used as a correlator in the CCK+DQPSK mode, the weights need to be adjusted such that the signal received by the correlator correspond to the appropriate signal stored in the correlator as a “prototype symbol”.

If, on the other hand, the FIR filter is used as a matched filter in the GFSK mode, the weights of two of the filters can be set to the appropriate impulse responses so that they match to the frequencies f_1 and f_2 and the remaining filters can be switched off using appropriate switches (not shown).

However, because the output from the redundant filters will be zero in GFSK mode, GFSK mode can alternatively be operated without switching off the remaining filters.

In this way the matched filter of FIR architecture described with reference to Figure 15 above can be used both as a correlator and as a matched filter depending on the filters weights. The weights of the combined correlators/filters 610 for the integrated demodulator are thus programmable.

An FIR architecture as shown in Figure 15 is suitable to be used as a module of the complex correlators 610 (i.e. similar to the modules of the correlators 210 described above with reference to Figure 11, where the outputs of both correlator modules for the real and the imaginary part are summed). In this way a complex correlator for the CCK+DQPSK mode is provided.

As an example, assume that the complex correlator is the last in the bank of 64. Then the weights on the inphase and quadrature braches are set to Z_{64} = +j-1-1+j-1-j+j+1. And if the 64^{th} CCK+DQPSK symbol (S_{64}) is received, then the output of the correlator is given by the expression in equation (2) below. No other correlator will have a greater output.

$$\text{Output} = (0x0 + (-1)x(-1) + (-1)x(-1) + 0x0 + (-1)x(-1) + 0x0 + 0x0 + 1x1) + (1x1 + 0x0 + 0x0 + 1x1 + 0x0 + (-1)x(-1) + 1x1 + 0x0) = 8 \qquad (2)$$

In GFSK mode, all the weights of 62 complex correlators 610 out of the 64 correlators are set to zero, and thus their outputs will always be zero. Alternatively, these 62 correlators 610 can be switched off using appropriate switches (not shown).

The remaining two correlators 610 have the weights on one of their arms (e.g. the quadrature arm) set to zero, reducing them to simple FIR filters. The weights on the remaining arm of one of these correlators are set to the appropriate impulse response that will match it to a signal frequency f_1. Similarly, the same procedure is repeated with the second complex correlator to match it to frequency f_2.

The outputs of the correlators 610 are fed into decision element 614 on lines 621 to 626. The output of the decision element 614 is then transmitted to logic circuit 618 on the six parallel lines 621 o 626.

When a signal reaches decision element 614, the element determines with the sampler and comparator which one of correlators 610 produces the greatest output and sends out a bit 1 on the output line associated with this correlator. Logic circuit 618 ensures that the output of the demodulator 600 is appropriate for both the GFSK and the CCK+DQPSK mode. Logic circuit 618 outputs the data word for CCK+DQPSK mode, and the data bit for GFSK

mode, is a suitable form. In CCK+DQPSK mode, there are 64 output possibilities, and in GFSK mode there are only 2 possible outputs.

A control of the modem switches between the two modulation techniques, i.e. the CCK+DQPSK and the GFSK mode. The integrated modulator then automatically sets all the appropriate switches (such as switch 550 and 605) and selects the according functions (for example in the serial-to-parallel converter 510, the FIR elements 610 and the logic circuit 618) such that the modem correctly modulates or demodulates data according to the selected modulation technique.

As the modem according to embodiments of the present invention is an integrated modem rather than two separate modems, which are combined as in the prior art described above, no inter working element is needed. This results from the fact that the integrated modem, i.e. the integrated modulator and the integrated demodulator, uses most of the individual elements or building blocks for both modulation or demodulation techniques.

Other Embodiments

In the foregoing an integrated modem architecture is described which is capable of modulating and demodulating signal in accordance with the CCK+DQPSK and the GFSK modulation technique.

It is appreciated that alternatively an integrated modem capable of modulating and demodulating in accordance with other modulation techniques can be used, like for example GFSK and QPSK, CCK+DQPSK and QPSK, GFSK and QAM QPSK and QAM or CCK+DQPSK and QAM.

In addition, integrated modems capable of modulating/demodulating according to more than two modulation techniques can be used.

The above described embodiment can for example be extended such that the modem is capable of modulating/demodulating three modulation techniques: CCK+DQPSK, GFSK and QPSK.

This can be implemented by again adjusting the timing, the use of additional switches (to switch off the differential demodulator and the DQPSK demodulator for the QPSK mode).

It is to be understood that the embodiments described above are preferred embodiments only. Various features may be omitted, modified or substituted by equivalents, without departing from the scope of the present invention.

Claims:

1. A modulating device for modulating and/or demodulating data for transmission from a first device to a second device, including modulating means capable of modulating and/or demodulating data according to at least a first and a second modulation technique using common digital modulation components.

2. A device according to claim 1, comprising a plurality of building blocks and wherein at least one of said building blocks are adapted to be used for modulating and/or demodulating data according to said at least first and second modulation technique.

3. A device according to claim 1 or 2, wherein said at least one building block comprises:

(a) a programmable finite impulse response filter;

4. A device according to claim 1 or 2, wherein said at least one building block comprises:

(b) a look-up table;

5. A device according to claim 1 or 2, wherein said at least one building block comprises:

(c) a serial-to-parallel converter.

6. A device according to claim 3, wherein said finite impulse response filters are programmable to a first and a second mode for said first and second function, respectively.

7. A device according to claim 6, wherein said finite impulse response filters are adapted to be used as correlators in a first mode.

8. A device according to claim 6 or 7, wherein said finite impulse response filters are adapted to be used as matched filters in a second mode.

9. A device according to any of claims 3 or 6 to 8, wherein said finite impulse response filters are adaptable by varying their weights.

10. A device according to claim 3, wherein said look-up table includes data related to said first and second modulation technique.

11. A device according to claim 10, wherein said look-up table comprises n input words, m output words relating to said first modulation technique and p output words relating to said second modulation technique, wherein $n \geq m$ and $n \geq p$.

12. A device according to claim 11, wherein n > p and wherein only p input words are used for determining output words related to said second modulation technique.

13. A device according to any preceding claim, comprising timing means adjustable to a first clocking time used for modulating/demodulating data according to said first modulation technique and a second clocking time used for modulating/demodulating data according to said second modulation technique.

14. A device according to claim 13, wherein said timing means comprises a serial-to-parallel converter.

15. A device according to any preceding claim, wherein said modulating means is adapted to automatically switch between said at least first and second mode.

16. A device according to any preceding claim, wherein said techniques are CCK+DQPSK and the GFSK modulation technique.

17. A device according to any of claims 1 to 15, wherein said techniques are the QPSK and the GFSK modulation technique.

18. A device according to any of claims 1 to 15, wherein said techniques are a frequency modulation technique and a quadrature modulation technique.

19. An electronic device adapted to communicate data to and/or from a second electronic device, the device comprising modulating means according to any preceding claim.

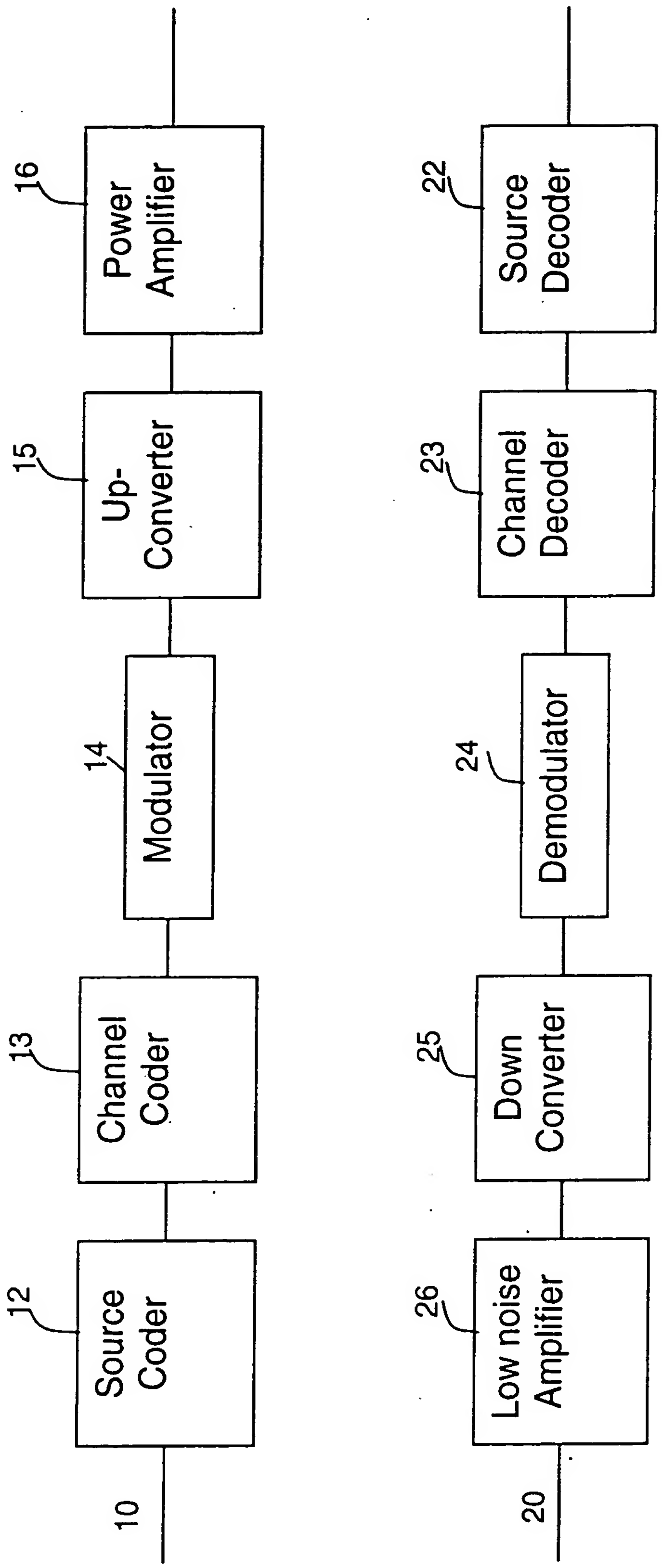
20. A method of adapting modulating means for modulating data for transmission from a first device to a second device and/or demodulating modulated data suitable for a first modulation technique such that said modulating means is capable for modulating and/or demodulating data according to at least a first and a second modulation technique, comprising providing a common digital modulation component used in both techniques.

21. A modulating means for modulating and/or demodulating data for transmission from a first device to a second device substantially as herein described with reference to the accompanying drawings.

Abstract

Integrated Modulators and Demodulators

A modulating means for modulating and/or demodulating data for transmission from a first device to a second device, wherein the modulating means is capable of modulating and/or demodulating data according to at least a first and a second modulation technique.



10
12
Source Coder
13
Channel Coder
14
Modulator
15
Up-Converter
16
Power Amplifier
20
26
Low noise Amplifier
25
Down Converter
24
Demodulator
23
Channel Decoder
22
Source Decoder

Fig. 1

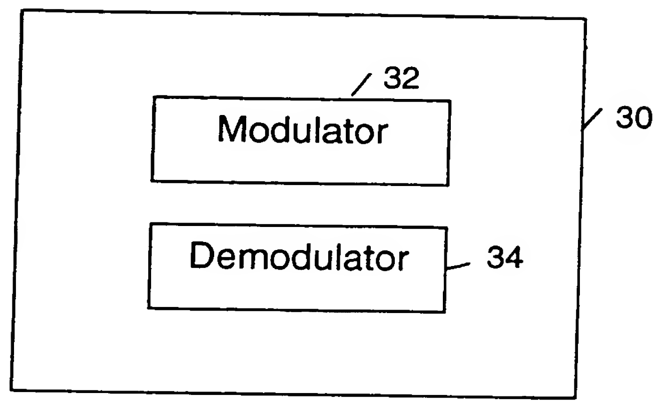

32
Modulator
30
Demodulator
34

Fig. 2

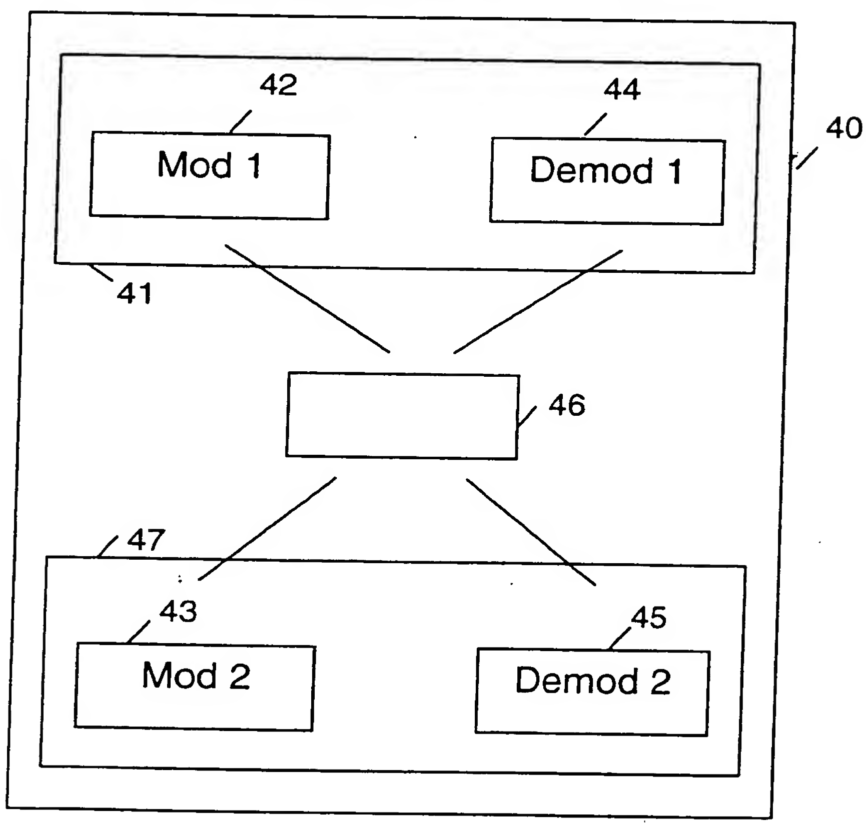
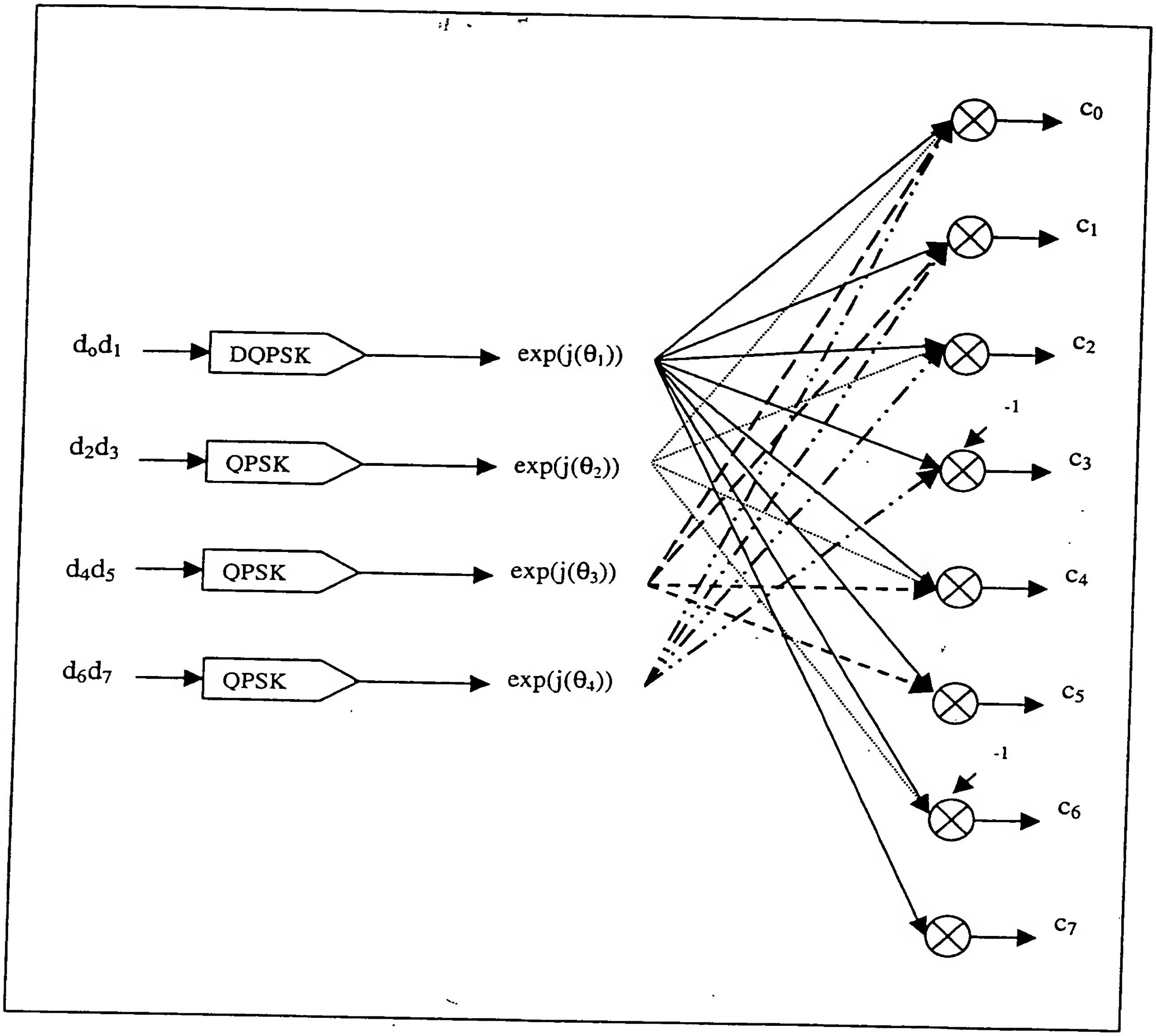

42
44
40
Mod 1
Demod 1
41
46
47
43
45
Mod 2
Demod 2

Fig. 3



d_0d_1
DQPSK
$\exp(j(\theta_1))$
d_2d_3
QPSK
$\exp(j(\theta_2))$
d_4d_5
QPSK
$\exp(j(\theta_3))$
d_6d_7
QPSK
$\exp(j(\theta_4))$
c_0
c_1
c_2
-1
c_3
c_4
c_5
-1
c_6
c_7

Fig. 4

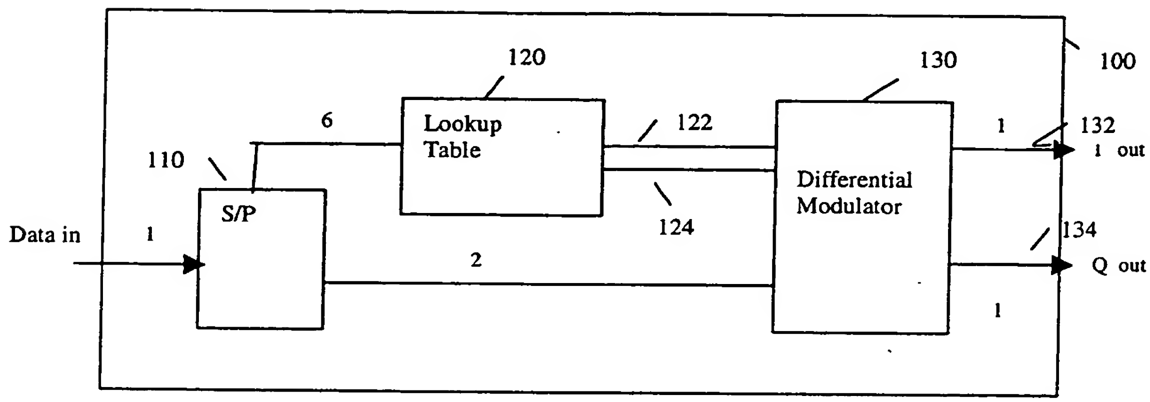

120
130
100
Lookup Table
122
1
132
I out
110
6
Differential Modulator
S/P
124
Data in
1
134
2
Q out
1

Fig. 5

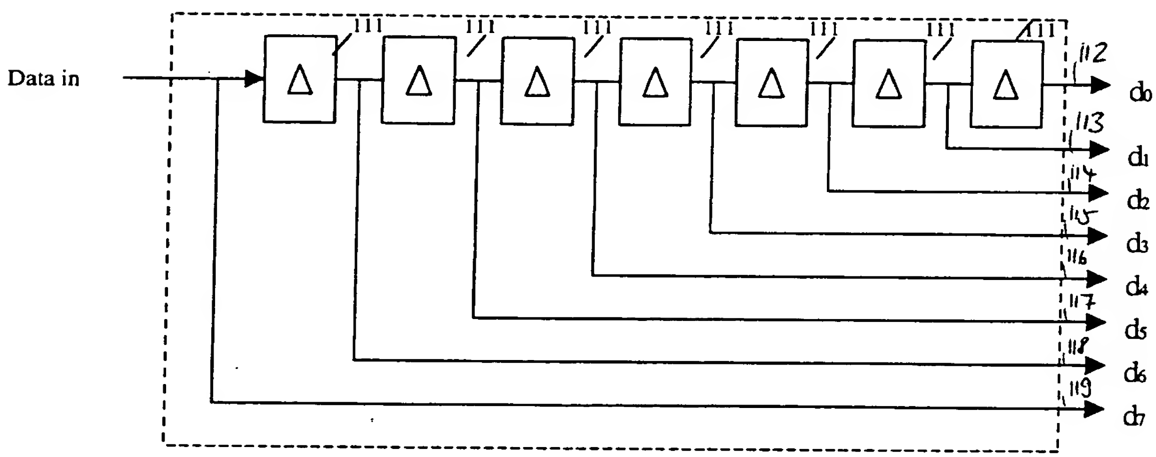

Data in
111
112
113
114
115
116
117
118
119
d_0
d_1
d_2
d_3
d_4
d_5
d_6
d_7

Fig. 6

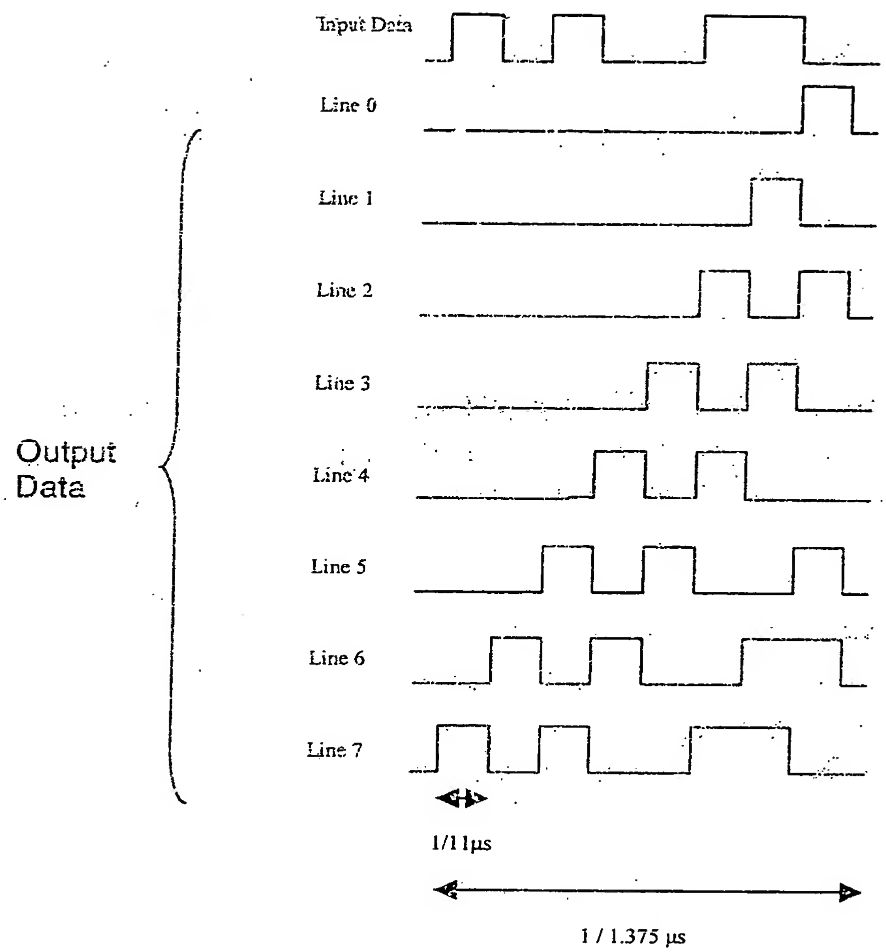

Input Data
Line 0
Line 1
Line 2
Line 3
Line 4
Line 5
Line 6
Line 7
Output Data
1/11µs
1 / 1.375 µs

Fig. 7

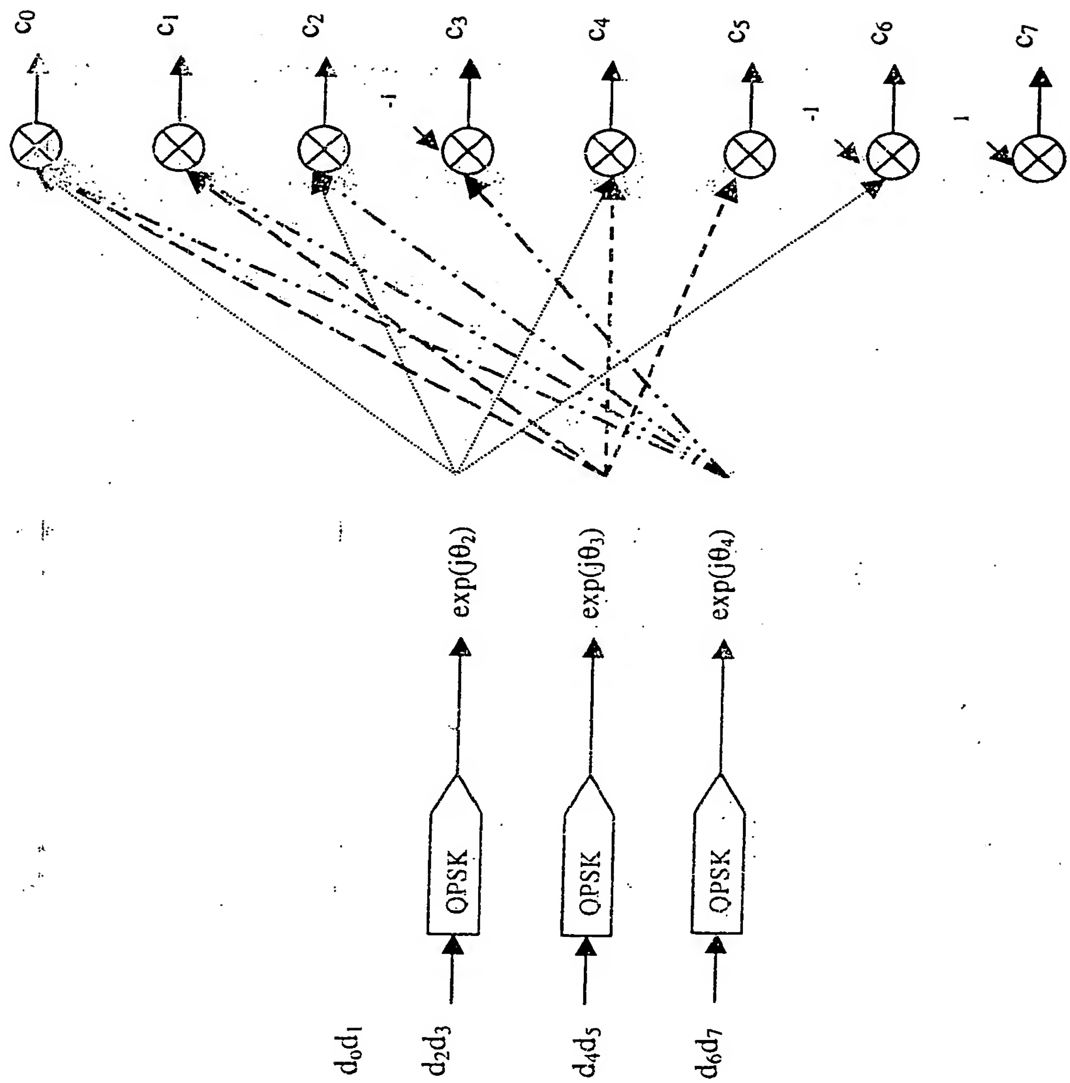
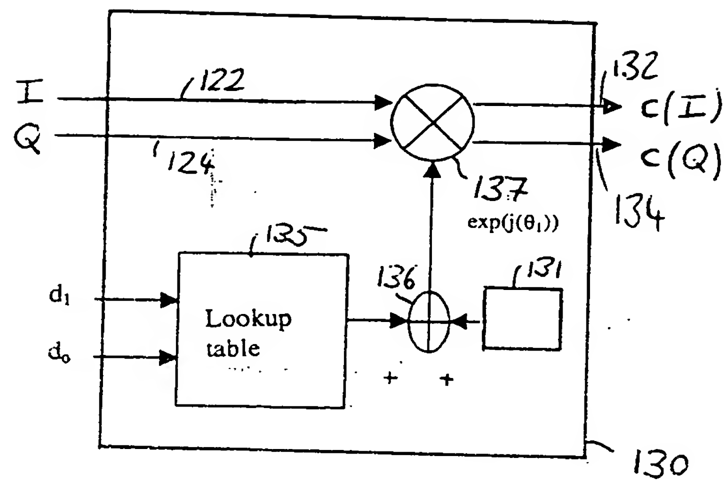
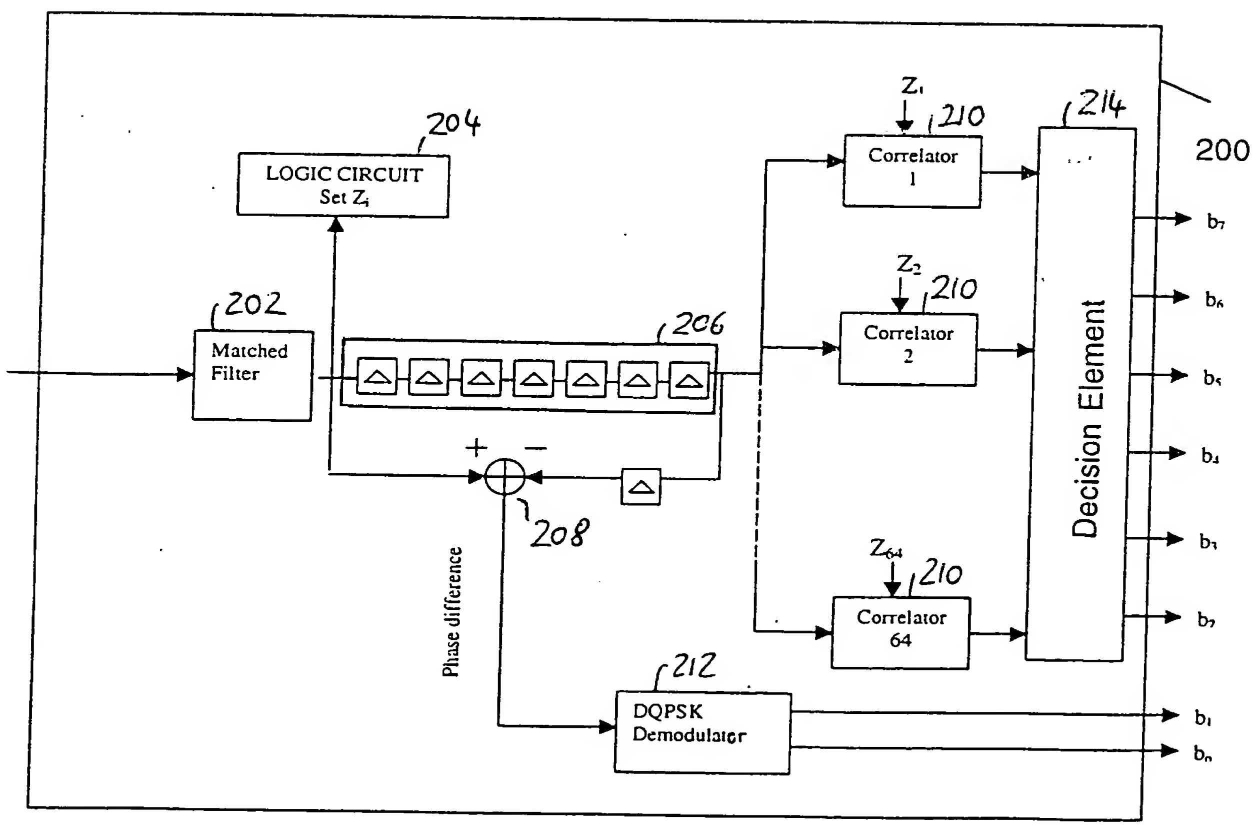

c_0
c_1
c_2
c_3
c_4
c_5
c_6
c_7
-1
-1
1
$\exp(j\theta_2)$
$\exp(j\theta_3)$
$\exp(j\theta_4)$
QPSK
QPSK
QPSK
d_0d_1
d_2d_3
d_4d_5
d_6d_7

Fig. 8



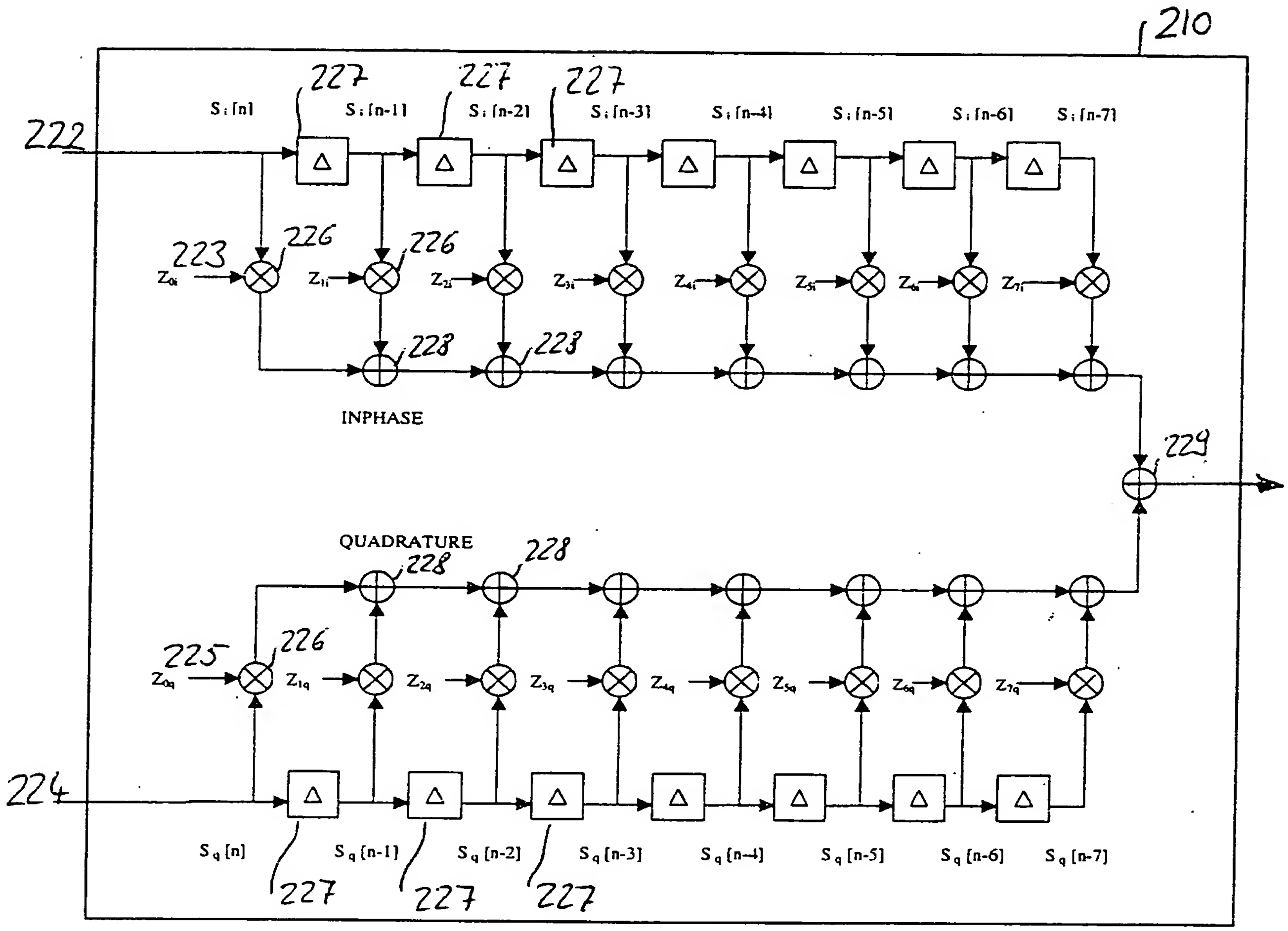
I
Q
122
124
132
c(I)
c(Q)
134
137
exp(j(θ1))
135
136
131
d1
d0
Lookup table
+
+
130

Fig. 9



200
204
LOGIC CIRCUIT
Set Zi
202
Matched Filter
206
+
−
208
Phase difference
212
DQPSK Demodulator
Z1
210
Correlator 1
Z2
210
Correlator 2
Z64
210
Correlator 64
214
Decision Element
b7
b6
b5
b4
b3
b2
b1
b0

Fig. 10



210
222
223
224
225
226
227
228
229
$S_i[n]$
$S_i[n-1]$
$S_i[n-2]$
$S_i[n-3]$
$S_i[n-4]$
$S_i[n-5]$
$S_i[n-6]$
$S_i[n-7]$
Z_{0i}
Z_{1i}
Z_{2i}
Z_{3i}
Z_{4i}
Z_{5i}
Z_{6i}
Z_{7i}
INPHASE
QUADRATURE
Z_{0q}
Z_{1q}
Z_{2q}
Z_{3q}
Z_{4q}
Z_{5q}
Z_{6q}
Z_{7q}
$S_q[n]$
$S_q[n-1]$
$S_q[n-2]$
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$S_q[n-6]$
$S_q[n-7]$

Fig. 11

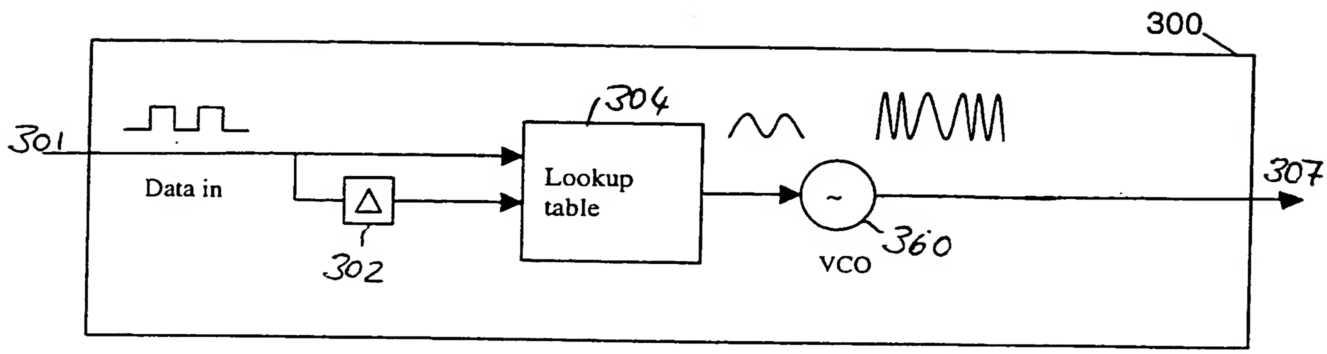

Fig. 12

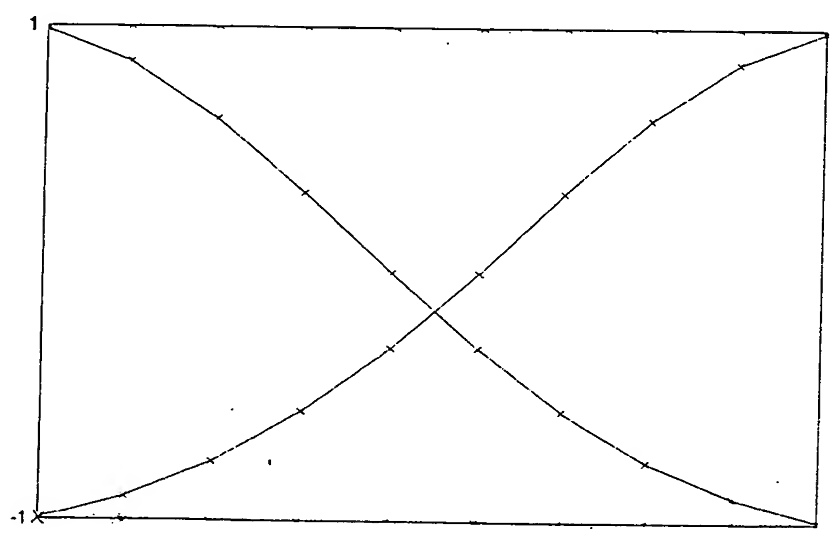

Fig. 13

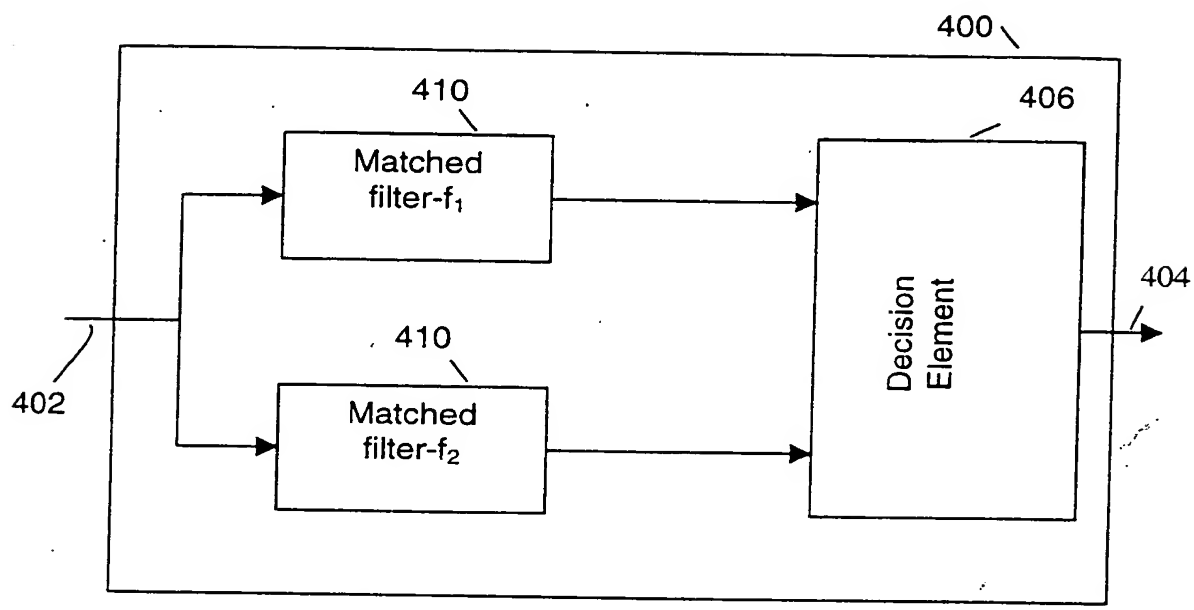
400
410
Matched filter-f_1
406
Decision Element
404
410
Matched filter-f_2
402

Fig. 14

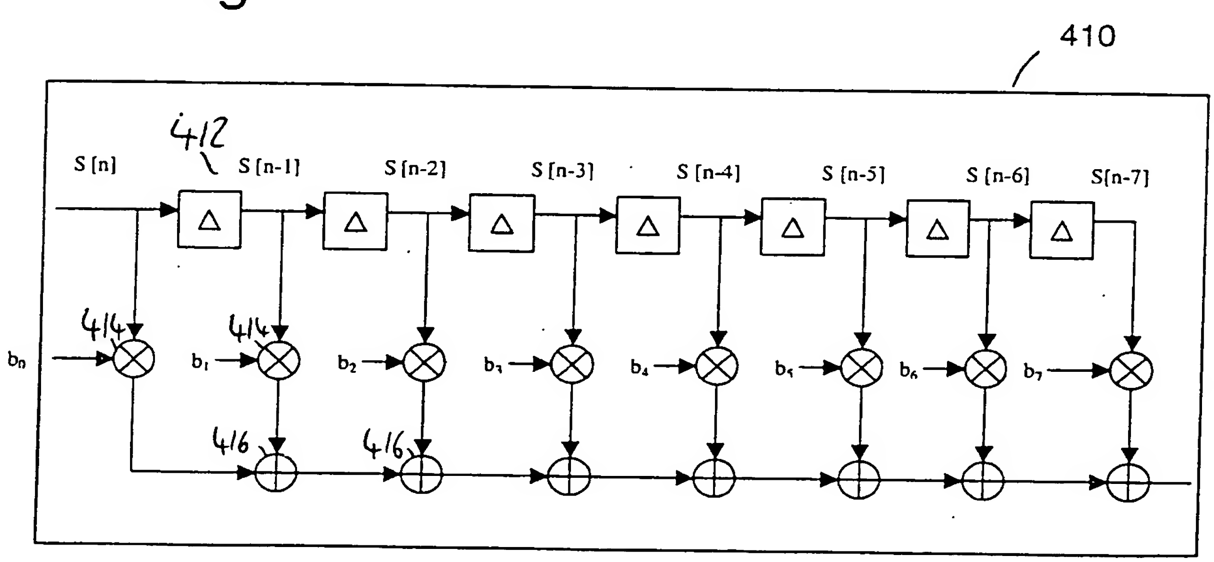
410
412
S[n]
S[n-1]
S[n-2]
S[n-3]
S[n-4]
S[n-5]
S[n-6]
S[n-7]
414
414
416
416
b_0
b_1
b_2
b_3
b_4
b_5
b_6
b_7

Fig. 15

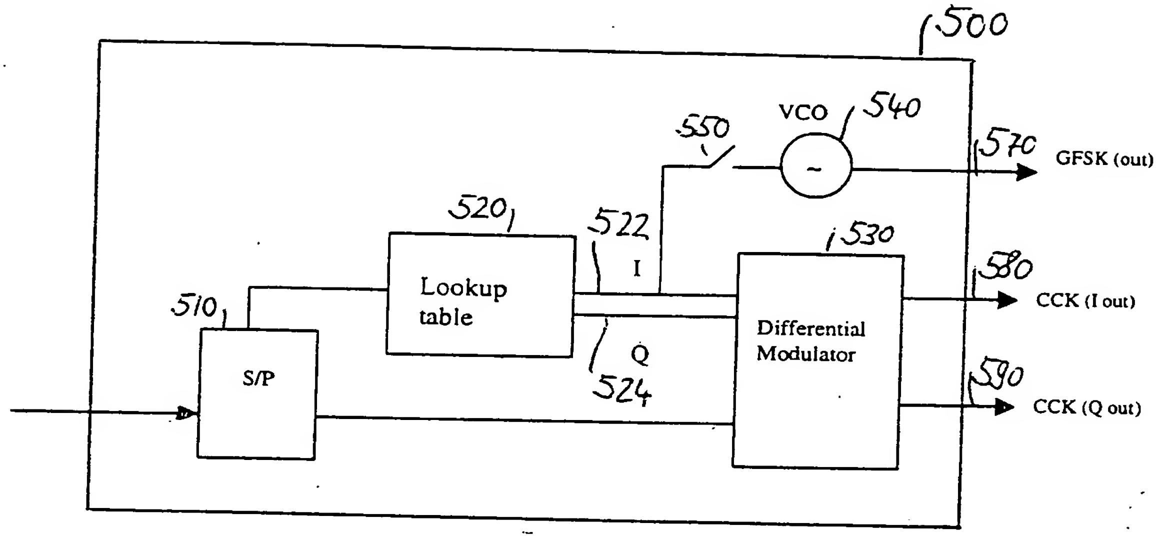
500
VCO
540
550
570
GFSK (out)
520
522
I
530
580
Lookup table
510
CCK (I out)
Differential Modulator
Q
S/P
590
524
CCK (Q out)

Fig. 16

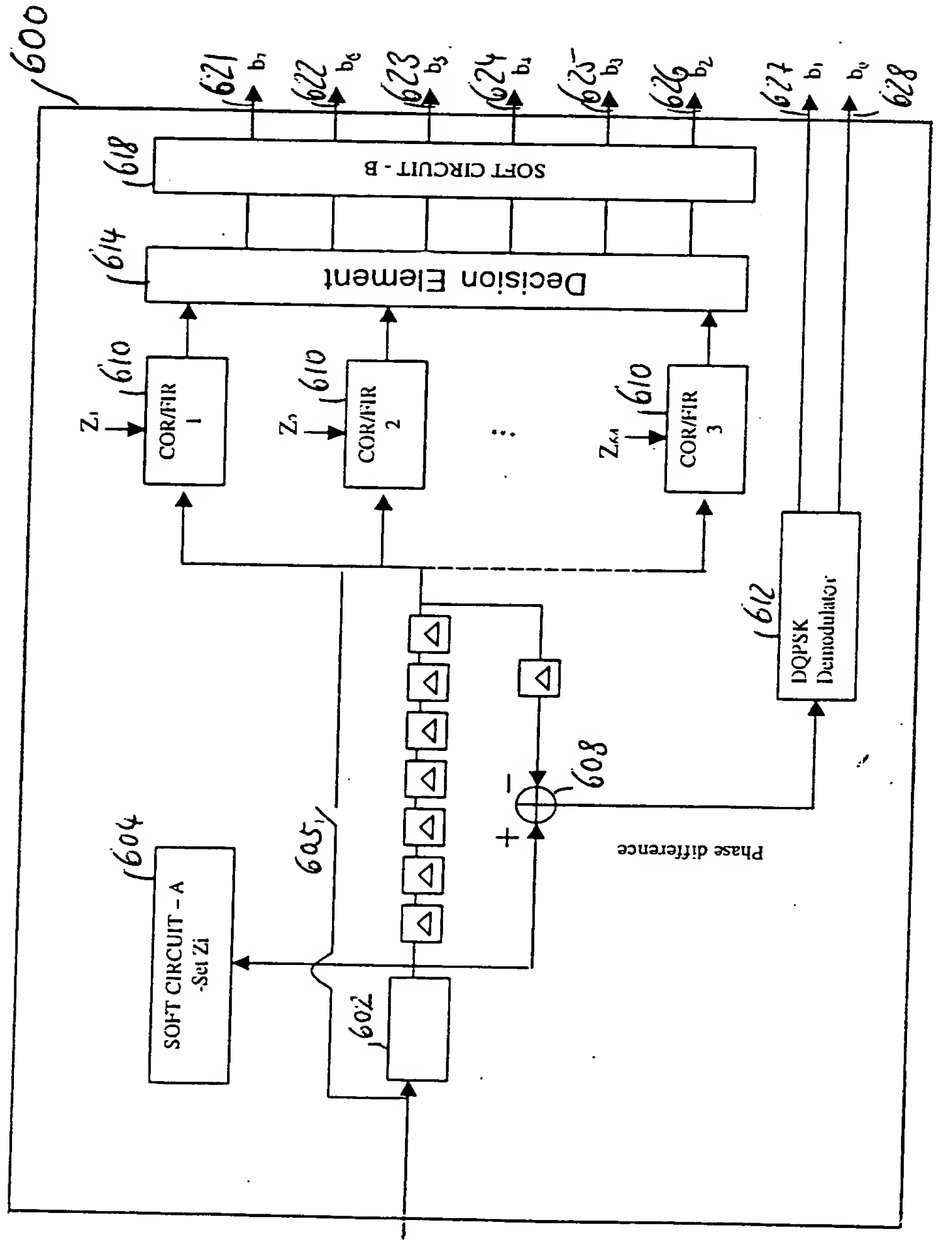
600
621
622
623
624
625
626
627
628
618
SOFT CIRCUIT - B
614
Decision Element
610
COR/FIR 1
COR/FIR 2
COR/FIR 3
612
DQPSK Demodulator
608
Phase difference
604
SOFT CIRCUIT – A -Set Zi
605
602

Fig. 17